

### **ABSTRACT OF THE DISCLOSURE**

In a preferred embodiment, the invention provides a circuit and method for a smaller and faster triple redundant latch. Three settable memory elements set an identical

5 logical value into each settable memory element. After the settable memory elements are set, a voting structure with inputs from the first settable memory element, the second memory element, and control to the settable memory elements determines the logical value held on the third settable memory element. The propagation delay through the third settable memory element is the only propagation delay of the triple  
10 redundant latch.